"NU4YOU": RISC-V Hands-On Workshop at Naresuan University
Date: June 28, 2023
Time: 13:00-16:00
Venue: Auditorium 4, King Naresuan the Great Exhibition and Convention Center (KNECC), Phitsanulok, Thailand
Instructor: Paul Sherman, RISC-V International Foundation

Discover the game-changing potential of RISC-V architecture at our exclusive workshop. Don't miss this opportunity to dive into the world of open-source instruction set architecture that's revolutionizing the industry.

In this workshop, you will get hands-on experience with RISC-V development tools and learn that RISC-V is rather fun, easy, simple, elegant, and no risk at all!

This workshop is brought to you by JCSSE2023 Conference and RISC-V International Foundation.

NU Setup:
- Six tables, each with 3-5 people
- A chalkboard or whiteboard nearby
- Six PCs (one per table)
- A 2-ch oscilloscope (portable)

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I'm bringing six sets of little hardware modules extremely easy to configure, install, and work with; each set is a LoFive-R1 board (RV32IMAC core and handy peripherals); an FT232R device for the USB-to-JTAG interface; a bunch of jumper wires; and will be given away to six lucky people who pull the winning number from the hat, or best answer our fun quiz questions (for example: whoever can give the best answer to the age old question: Is 'firmware' part of 'hardware' or 'software'?). I am also bringing my pre-configured Raspberry PI, for those brave workshop souls who wish to bitbang JTAG and not use USB :)
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Workshop format:
- 30 Minutes for introduction and general description to the world of RISC-V
- 1 1/2 to 2 Hours for the hands-on-workshop breakout into the six groups
- 30 Minutes for summary, closure, and review of each table's explorations

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Each workshop table will be dedicated to exploring one aspect of RISC-V; we can give each table a fun name, suggested in parentheses; I will provide paper handouts for each of these mini-lessons for people to type in and try.
--- Table 1: RV32A ("The Atomics"): load-mod-store; amoxxx; memory alignment; rd before the mod

--- Table 2: RV32U ("The Privileged"): user, supervisor, hypervisor, machine modes; interrupts & exceptions; vector tables & alignments; enabling and clearing pending bits; CLINT & PLIC
--- Table 3: RV32C ("The Compressed"): half size but fewer registers; how to force; how to prevent use of
--- Table 4: RV32M ("The Math"): multiply & divide; rem instruction as modulus; no subtract-immediate!
--- Table 5: RV32I ("The Base"): arithmetic & logic instructions; carry & borrow; immediate & register instruction forms; long-immediate & short-immediate; lui & auipc; The Wonderful 'O'; conditional & unconditional jump
--- Table 6: Toolchain ("The Assemblers"): compile, assemble, link, load, debug; gnu, git, and (Xe)(La)(TeX); how & where to get, all for free, and how to 'build' all tool programs from scratch
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